Amendments to the Claims

This listing of claims replaces all prior versions, and listings, of claims.

Listing of Claims

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1. (Currently Amended) An electrically programmable transistor fuse having a substrate of semiconductor material of a first conductivity type, a source region and drain region disposed in said substrate and spaced apart to define a substantially continuous channel region of monolithic substrate material therebetween, and a layer of insulating material having a uniform thickness and disposed over said source region, drain region and channel region, said electrically programmable transistor fuse comprising:

a first gate and a second gate disposed in a single layer of polysilicon over said insulating material, said first gate disposed overlapping a portion of said source region and said second gate electrically isolated from said first gate and disposed overlapping a portion of said drain region, wherein said first gate includes a terminal for receiving an externally applied signal and said second gate is capacitively coupled to said drain region; and

a coupling device disposed within said substrate and adapted to increase capacitive coupling of said second gate and said drain region, wherein programming is effectuated by charging said second gate via capacitive coupling with said drain region.

2. (Original) The fuse of Claim 1, wherein said programming is effectuated via application of a voltage signal to said drain region and said voltage signal is less than junction breakdown of said transistor fuse.

3. (Original) The fuse of Claim 1 further comprising an extended width drain portion integral with said drain region disposed in said substrate overlapping said second gate for increasing capacitive coupling.

4. (Original) The fuse of Claim 1 further comprising an extended width drain portion integral with said drain region disposed in said substrate overlapping a portion of said second gate and a well region disposed in said substrate also overlapping a portion of said second gate, wherein said well region is isolated from said second gate and said drain.

5. (Original) The fuse of Claim 4, wherein programming is effectuated by providing a ground reference to said source, the transistor threshold voltage to said first gate, and a program voltage to said drain region and said isolated well region.

6. (Original) The fuse of Claim 5, wherein said program voltage is less than the transistor junction breakdown.

7. (Original) The fuse of Claim 5, wherein reading is effectuated by providing a reference voltage to said first gate and detecting current flow between said source region and said drain region, wherein a programmed state is determined when no current is detected and a non-programmed state is determined when current is detected.

8. (Original) The fuse of Claim 7, wherein said reference voltage is greater than the transistor threshold voltage.

9. (Original) The fuse of Claim 5, wherein reprogramming is effectuated by providing the inverse of said programming voltage to said first gate.

10. (Currently Amended) A programmable fuse cell having a substrate of semiconductor material of a first conductivity type, a source region and drain region disposed in said substrate and spaced apart to define a substantially continuous channel region of monolithic substrate material therebetween, and a layer of insulating material having a uniform thickness and disposed over said source region, drain region and channel region, said transistor fuse comprising:

a transistor fuse comprising:

a first gate and a second gate disposed in a single layer of polysilicon over said insulating material, said first gate disposed overlapping a portion of said source region and said second gate isolated from said first gate and disposed overlapping a portion of said drain region;

said first gate includes a terminal for receiving an externally applied signal and said second gate is capacitively coupled to said drain region; and

a coupling device disposed within said substrate and adapted to increase capacitive coupling of said second gate and said drain region, wherein programming is effectuated by charging said second gate via capacitive coupling with said drain region; and

first circuitry coupled to said first gate terminal and adapted for selecting said transistor fuse for programming via a voltage signal; and

second circuitry coupled with said drain region and said coupling device and adapted for programming and reading the programming state of said transistor fuse.

11. (Previously Presented) The fuse cell of Claim 10, wherein said second circuitry includes a further transistor coupled with said drain region and said coupling device for delivering a programming voltage signal when selected on.

12. (Previously Presented) The fuse cell of Claim 11, wherein said second circuitry includes further circuitry coupled with said transistor fuse for detecting current flow therein when said further transistor is selected off.

13. (Original) The fuse cell of Claim 10, wherein said programming is effectuated via application of a voltage signal to said drain region and said coupling device which is less than junction breakdown of said transistor fuse.

14. (Original) The fuse cell of Claim 10, wherein said transistor fuse further comprises an extended width drain portion integral with said drain region disposed in said substrate overlapping said second gate for increasing capacitive coupling.

15. (Original) The fuse cell of Claim 10, wherein said transistor fuse further comprises an extended width drain portion integral with said drain region disposed in said substrate overlapping a portion of said second gate and a well region disposed in said substrate also overlapping a portion of said second gate, wherein said well region is isolated from said second gate and said drain.

16. (Original) The fuse cell of Claim 10, wherein programming is effectuated by providing a ground reference to said source, the transistor threshold voltage to said first gate via said first circuitry, and a programming voltage to said drain region via said second circuitry.

17. (Original) The fuse cell of Claim 16, wherein said program voltage is less than the transistor junction breakdown.

18. (Original) The fuse cell of Claim 16, wherein reading is effectuated by providing a reference voltage to said first gate via said first circuitry and detecting current flow between said source region and said drain region via said second circuitry, wherein a programmed state is determined when no current is detected and a non-programmed state is determined when current is detected.

19. (Original) The fuse cell of Claim 18, wherein said reference voltage is greater than the transistor threshold voltage.

20. (Previously Presented) The fuse cell of Claim 16, wherein reprogramming is effectuated by providing a voltage of opposite polarity to the programming voltage to said first gate via said first circuitry.